Even and Odd Parity Generator and Checker using the Reversible logic gates

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Abstract— Digital data transmission is the mostly used in the communication. The data transmission from source to destination should be without loss of information. This is made possible by using the method of parity generator and parity checker. The parity checker and the parity generator are of two types they are even parity generator and parity checker, odd parity generator and checker. Reversible logic gates compremises various parameters in the data transmission. There are various reversible logic gates to meet the needs of the parity generator and parity checker. Reversible gates probably reduce the number of gates utilised in the conventional method. The Parity generator and the parity ckecker is effective method to find the error in the destination end. The reversible logic gate called Feynman gate is used in the process which make the data transmissionmuch more effective with no data loss and is simulated using the simulator 'Modelsim'.

Index Terms: Parity generator, parity checker, Reverversible logic, Feynman gate

I. INTRODUCTION

THE parity generator is the method to chek the error present while transmitting data from the transmitter node to the receiver node. Parity generator is of two types they are odd parity generator and the even parity generator. The reversible logic gates are used in the generation of the parity generator and for the parity checker. This is done using the reversible logic gates since the reversible logic gates are non- information loss gates. This parity generating technique is the most efficient technique and is one of the most widely used in the error detection techniques for the data transmission. This generation and the checking of the parity of the bits are performed by the method of the reversible logic gate makes the data transmission much easier than the conventional methods. This use of the reversible logic gates reduces the loss of information, delay and the number of gates used. Reversible logic enables the circuit to perform the retival of the information easily by using the garbage values in the reversible gates.

II. REVERSIBLE LOGIC

The reversible logic has one to one mapping between the input and the output vectors. The reversible gates do not loose any information and the input and the output are uniquely retrievable from each other. The reconstruction of the input data is made possible from the output and the garbage vectors at output state. The reversible logic gate effectively reduces the heat dissipation and hence the loss of information is reduced and thereby allows higher densities and higher speed. These gates reduce the complexity of implementation and works in a single clock pulse. The reversible logic Gates have zero fan-out and hence the power dissipation is also zero [1]. The reversible logic has garbage values along with the output terms. The relation between the input, output and the garbage value is as below [2]

Input + Constant Input = Output + Garbage

Quantum cost, garbage, constant input, delay are the main parameters to be discussed on the reversible logic. Delay calculation is an essential feature of every circuit to manipulate the efficiency. It is denoted by Δ. Quantum cost of a circuit is mainly based on the number of quantum gates present in the circuit.

The calculation of the Quantum cost is done by using the gate whose quantum cost is known and finally adding up all the quantum cost of the gates present in the circuit [3]. Each and every gate produces the output which is not used for the further synthesis and those left out outputs are called the 'garbage'. Although the garbage values are not used for the further synthesis they are essential to achieve the reversibility. The constant inputs are the 0's and 1's. The constant input terms are also called as ancilla input bit [4].

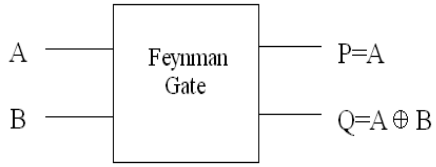

Fig. 1. Reversible Feynman Gate

The reversible logic gate used in this paper is the Feynman gate and this gate has the quantum cost of about 1.

III. PARITY GENERATOR

Parity bits are extra signals which are added to a data word to enable error checking. There are two types of Parity - even and odd. An even parity generator will produce a logic 1 at its output if the data word contains an odd number of ones. If the data word contains an even number of ones then the output of the parity generator will be low.

A	B	C	OUTPUT (P)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table. 1. Even parity generator truth table

The truth table for the odd parity generator bit is given by the table below:

A	B	C	OUTPUT (P)
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Table. 2. Odd parity generator truth table

By concatenating the Parity bit to the data word, a word will be formed which always has an even number of ones i.e. has even parity. Parity is used on communication links (e.g. Modem lines) and is often included in memory systems. If a data or a word is sent out with even parity, but has odd parity when it is received then the data has been corrupted and must be resent. As its name implies the operation of an Odd Parity generator is similar but it provides odd parity. Even parity bit is given by the expression P = A xor B xor C. The even parity bits generation is given as shown in the above tables.

And the expression for the generation of the odd parity generator is given by P = A xor B xor C.

The even parity checker is shown in the truth table shown below:

A	B	C	Pin	OUTPUT (P)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Table.3 Even parity checker truth table

And the expression for the generation of the odd parity generator is given by P = A xor B xor C xor Pin.

The odd parity checker is shown in the truth table shown below:

A	B	C	Pin	OUTPUT (P)
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Table. 4. Odd parity checker truth table

And the expression for the generation of the odd parity generator is given by P = A xor B xor C xor Pin.

IV. Simulation and Discussion

The output of the even and odd parity generator and the parity checker is obtained by using the 'Modelsim' Simulator is as given below:

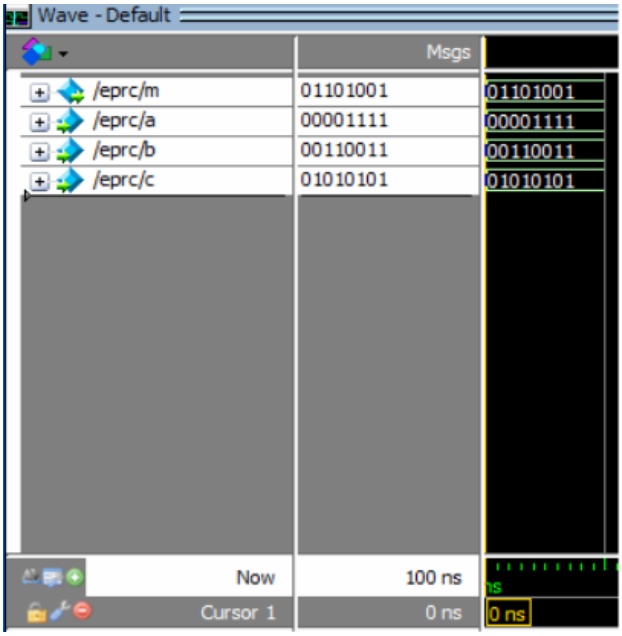

Fig. 2. Even parity generator simulation

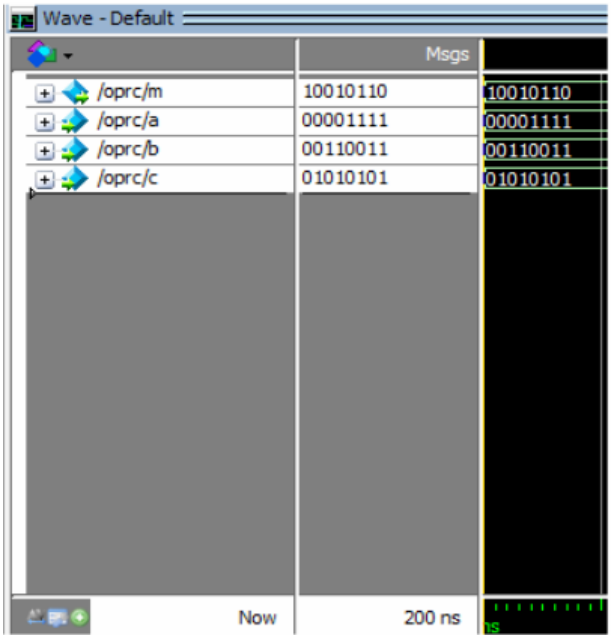

Fig. 3. Odd parity generator simulation

Parity generator	Number of Feynman gates	Garbage value
Even	16	16
Odd	24	16

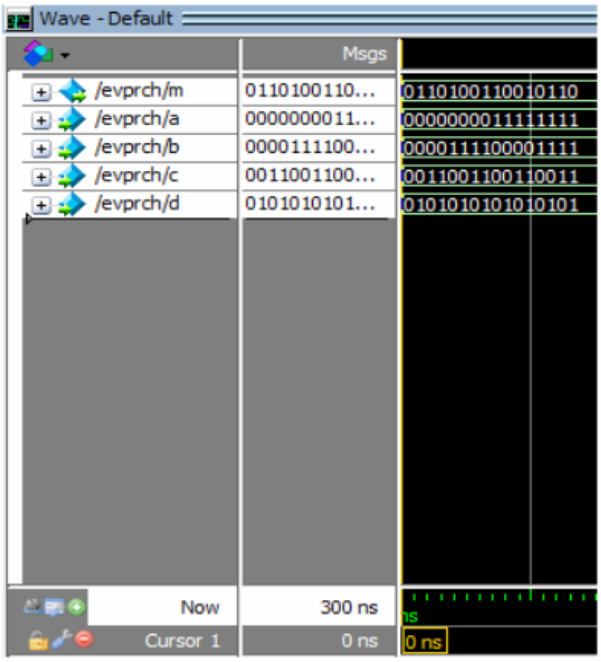

Fig. 4. Even parity checker simulation

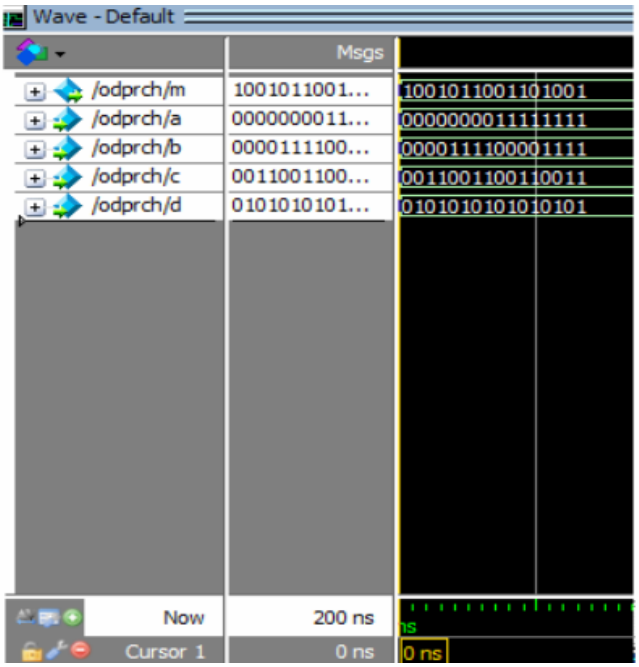

Fig. 5. Odd parity checker simulation

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Parity checker	Number of Feynman gates	Garbage value
Even	48	48
Odd	64	48

V. CONCLUSION

Thus the retiving of the data from the input data is made easy and more efficient while performing wit the reversible logic gates. The use of Feynman gate for parity generator and the parity checker with reduced power dissipation. The retival of the input data from the output so generated is made highly possible by the use of the garbage values.Hence reversible logic gates are effective than the conventional methods for efficient data transmission. The loss of information is zero in case of using the reversible logic gates for the data transmission in the digital form.

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