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Design and Analysis of Adiabatic Logic Based Frequency Divider

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Abstract- Frequency dividers are crucial circuits that are employed in PLLs and high-speed serialize/deserializers. The flip-flop-based frequency dividers are comprised of two D latches in cascade, and in a negative feedback configuration. The digital operation of this type of dividers provides the advantage of suppressing the sensitivity to waveform distortions. Furthermore, the flip-flop-based dividers achieve a wide bandwidth than other types of frequency dividers at low-to-medium range of frequencies. This paper presents a high-speed DFAL flip-flop-based frequency divider incorporating a new high-speed latch topology, which provides satisfactory performance for frequencies up to 17 GHz. This circuit is designed and simulated in a standard 0.18μm CMOS process. This architecture is primarily a master-slave flip-flop with a negative feedback. Thus frequency division is achieved. The designed circuit and the verification can be done in TANNER EDA.

Keywords- *adiabatic, digital circuit, DFAL, frequency divider, low power, stacking technology*.

I INTRODUCTION

With the advances in VLSI technology, there is a great demand of portable devices that perform high speed computing and support multimedia applications. However, the increased functionality and high speed operation result in high power dissipation which eventually creates a need for low power design solutions. Different solutions both at the architectural and structural levels have been suggested. One possible approach is to adopt adiabatic logic style over conventional CMOS logic style for circuit design. Adiabatic logic style is more energy efficient than the conventional CMOS logic style [10]. A number of families based on adiabatic logic style have been proposed in literature. The common adiabatic logic families that are frequently used are 2PADCL, ECRL, ADL, QSER and GFCAL. The mentioned logic families however suffer from the drawbacks of amplitude degradation, large time delays and circuit complexity. In this paper a DFAL based frequency divider using stacking technology is proposed.

II DFAL OVERVIEW

The common adiabatic logic families suffer from amplitude degradation, large time delays and circuit complexity. These drawbacks can be eliminated by using DFAL style. The DFAL style removes the diode from the charging and discharging path to overcome the above disadvantages. basic structure of a DFAL inverter is shown in Fig. 1a.The transistors M1, M2 implement the inverter.

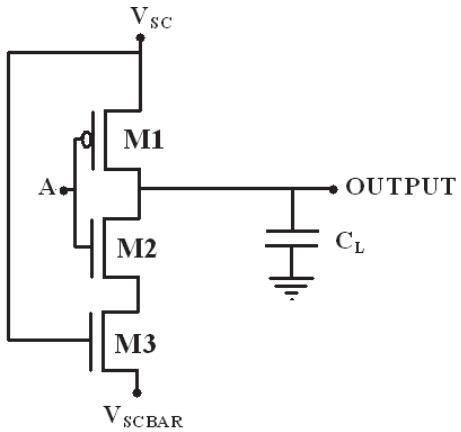

Fig 1a. DFAL Inverter

The transistor M3 is added in series with the transistor M2 for discharging and recycling of the output node charge. Its usage reduces the power dissipation significantly because it acts as a low value resistance, as compared to other adiabatic logic families which use diodes in the discharging path. The DFAL inverter employs spilt level sinusoidal power clock, as given in Fig.1b.

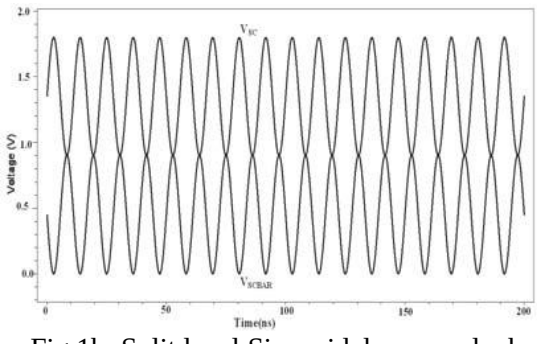

Fig 1b. Split level Sinusoidal power clock

This clock, in comparison to ramp or sinusoidal waveform, abates power dissipation, delay and degradation in output amplitude swing. In spilt level sinusoidal power clock, two clocks named VSC and VSCBAR are used respectively and VSCBAR differ by VDD/2 which helps in improving the performance of the logic family [8]. The operation of the DFAL inverter can be divided into two phases namely evaluation phase and hold phase, depending upon the supply clock phases. In the evaluation phase, the VSC makes a positive transition while VSCBAR makes a negative transition. Conversely, in the hold phase, the clocks VSC and VSCBAR makes negative and positive transitions respectively. In the evaluation phase, for a LOW value of the input A the transistor M1 is turned ON. If the output node Q is at the LOW value then the load capacitance □□ is charged via M2 resulting in the HIGH output state. Conversely, if the input A is HIGH the transistor M2 is turned ON and if at the same time output node Q is HIGH, then the discharging and recycling of output node charges to the power clock (VSCBAR) takes place ,via M2 and M3, causing the output to be LOW. In the hold phase no transition at the voltage level at the output node occurs. Therefore, the output node remains in the LOW state even if the nMOS network is ON. Similarly, the output continues to be in the HIGH state when the pMOS network is ON. Therefore, in the hold phase, as the switching activity at the output node is reduced, the power dissipation is significantly lowered.

III FREQUENCY DIVIDER

In modern integrated transceivers operating at microwave frequencies, one of the most critical parts is the frequency divider chain of the PLL frequency synthesizer. Being the VCO output frequency in the order of several GHz, the problem of actually implement the frequency division at such high frequencies is a non trivial one. In fact, depending on the frequency that needs to be divided, different approaches can be used.

The simplest way to implement a clock frequency division is to design a digital counter, it a digital logic resetting the counter after a number of input clock cycles equal to the division ratio have been counted. The drawback of this kind of solution is the limited maximum frequency of operation due to the digital logic with which the counter is implemented. Usually, such a frequency divider will operate up to few GHz (typically no more than 3-4 GHz). On the other side, such a frequency divider has the advantage of low power consumption, and the possibility of being programmable by dynamically changing the resetting logic (and thus the division ratio).

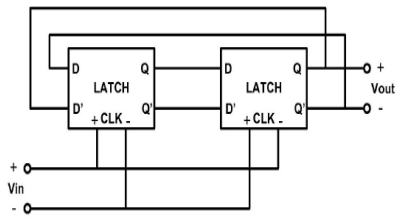

Fig 1.3 Master-Slave frequency divider block diagram.

When a higher frequency division is necessary, a purely analog solution has to be taken into consideration. The two main solutions to multi-GHz frequency division are: master-slave (MS) latch divider, and injection-locking divider (ILD). The MS divider employs a two stage regenerative divider. The ILD solution, instead, exploits the injection pulling effect on a VCO tuned at a frequency the half of the injected one. A possible implementation for the ILD is by means of a cross-coupled LC-tank VCO. To the extent of injecting the input differential signal, a NMOS-PMOS couple is used across the output terminal of the VCO.

In actual millimetre-wave PLL frequency synthesizers, a possible approach is to employ an ILD for the very first stage of the frequency divider chain (being the one operating at the highest frequency), and to use MS divider stages until the frequency is scaled down to values (3-4 GHz) at which a fully digital frequency divider can be used. The drawback of this kind of solution is the limited maximum frequency of operation due to the digital logic with which the counter is implemented. Usually, such a frequency divider will operate up to few GHz (typically no more than 3-4 GHz).

The digital frequency divider is indicated as a programmable divider, thus allowing a frequency channel selection capability. It is straightforward to understand that, the highest the maximum frequency of operation of the programmable frequency divider, the smaller the number of ILD/MS frequency divider stages [10].

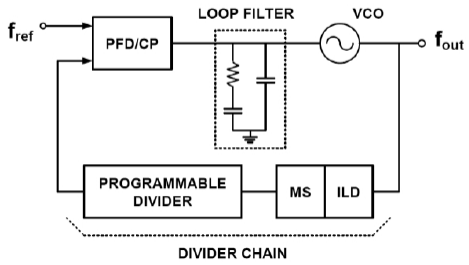

Fig 1.4 Millimetre-wave PLL frequency synthesizer architecture.

Moreover, the lower the number of high frequency divider stages, the lower the power consumption as well. Therefore, it is in the interest of the designer to maximize the maximum operating frequency of the digital frequency divider portion of the divider chain, in order to achieve a lower power consumption of the overall PLL[6]. Moreover, a digital frequency synthesizer can be implemented using standard-cell libraries and dedicated computer aided design (CAD) tools allowing a minimization of the layout area and a verification of the timing constraints.

IV PROPOSED SYSTEM

STACKING (CMOS) technology provides low leakage and high performance operation by utilizing high speed, low Vt transistors for logic cells and low leakage, high Vt devices as sleep transistors. Sleep transistors disconnect logic cells from the power supply and/or ground to reduce the leakage in sleep mode. In this technology, also called power gating, wake up latency and power plane integrity are key concerns. Assuming a sleep/wake up signal provided from a power management unit, an important issue is to minimize the time required to turn on the circuit upon receiving the wake up signal since the length of wake up time can affect the overall performance of the VLSI circuit.

Furthermore, the large current flowing to ground when sleep transistors are turned on can become a major source of noise on the power distribution network, which can in turn adversely impact the performance and/or functionality of the other parts of the circuit. In this paper we introduce an approach for reducing the transition time from sleep mode to active mode for a circuit part while assuring power integrity for the rest of the system by restricting the current that flows to ground during the transition.

The problem is to minimize the wakeup time while constraining the current flowing to ground during the sleep to active mode transition. Our approach is comprised of the following steps. First the discharge patterns of all logic cells are obtained. Next all cells in the circuit are clustered to a minimum number of clusters in such a way that the total discharge current of each cluster does not exceed a given threshold.

Another constraint is imposed on clustering which will prevent flowing of short circuit current during wakeup time. This constraint is handled by introducing a constraint graph and not allowing two cells with an edge between them in the same cluster. Finally for each cluster a single sleep transistor is assigned which is associated with a limited performance penalty and for each sleep transistor, a sleep/wake up signal is assigned. The wakeup times for the clusters are optimized to achieve minimum wake up time while maintaining a given threshold on overall discharge current.

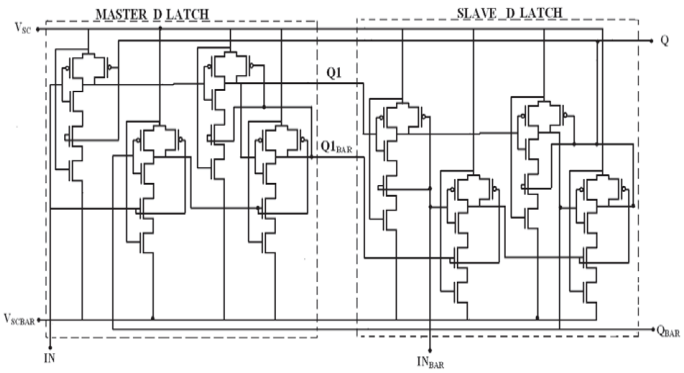

Fig 1.5 Proposed Circuit

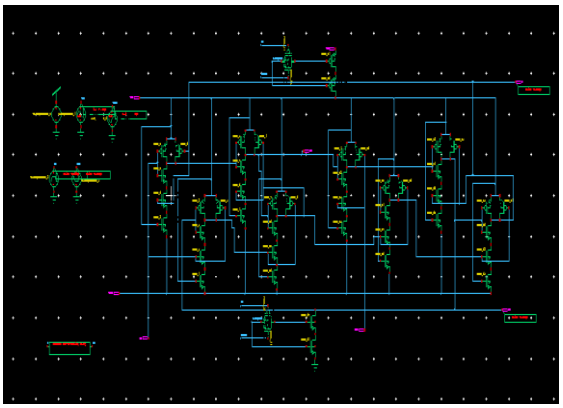

Fig 1.6 Schematic Diagram of Frequency divider using stacking technique

In this work, the focus will be on the implementation of a programmable Frequency divider featuring divide-by-24-25-26-27 division ratios. The architecture of the frequency divider is made up of four frequency divider chains. The desired division ratio is then selected by mean of an output multiplexer controlled by two control bits.

V RESULTS

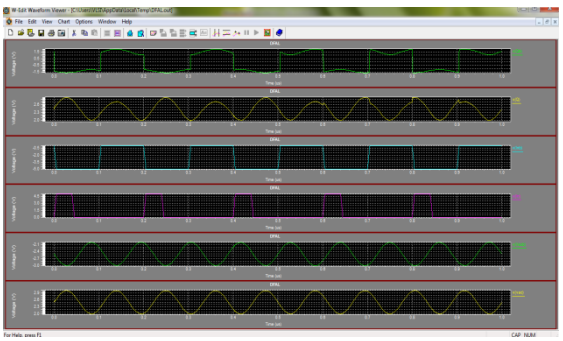

Fig 1.7 Output Waveform

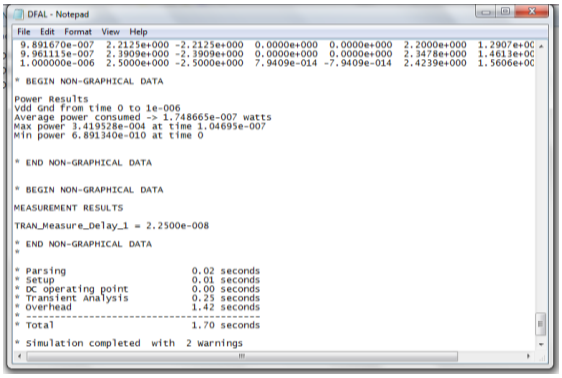

Fig 1.8 Power and Delay outputs

VI CONCLUSION

Thus, by implementing the stacking technique we reduced the total leakage of the circuit and also the time delay. This will improve the performance of the circuit and also the operation speed. Since we used a master slave architecture will give a regenerating effect.

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