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Fault Secure Memory Using Modified Decimal Matrix Code

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ABSTRACT: Transient multiple cell upsets (MCUs) are becoming major issues in the reliability of the memories exposed to radiation environment. To prevent the MCUs from causing data corruption, more complex error correction codes (ECCs) are widely used to protect memory, but the main problem is that they would require higher delay overhead. Recently, matrix codes (MCs) based on Hamming codes have been proposed for the memory protection. The main issue is that they are the double error correction codes and the error correction of the capabilities are not improved in all cases. In this paper, novel decimal matrix code (DMC) based on divide-symbol is proposed to the enhance memory reliability with lower delay overhead. The proposed DMC utilizes decimal algorithm to obtain the maximum of the error detection capability. Moreover, the encoder-reuse technique (ERT) is proposed to minimize the area overhead of the extra circuits without disturbing the whole encoding and the decoding processes .the ERT uses DMC encoder itself to be part of the decoder. The proposed of DMC is compared to the well-known codes such as the existing Hamming, MCs, and punctured difference set (PDS) codes. The only of the drawback to the proposed scheme is that it requires the more redundant bits for memory protection.

Index Terms—Decimal algorithm, error correction codes (ECCs), mean time to failure (MTTF), memory, multiple cells upsets (MCUs).

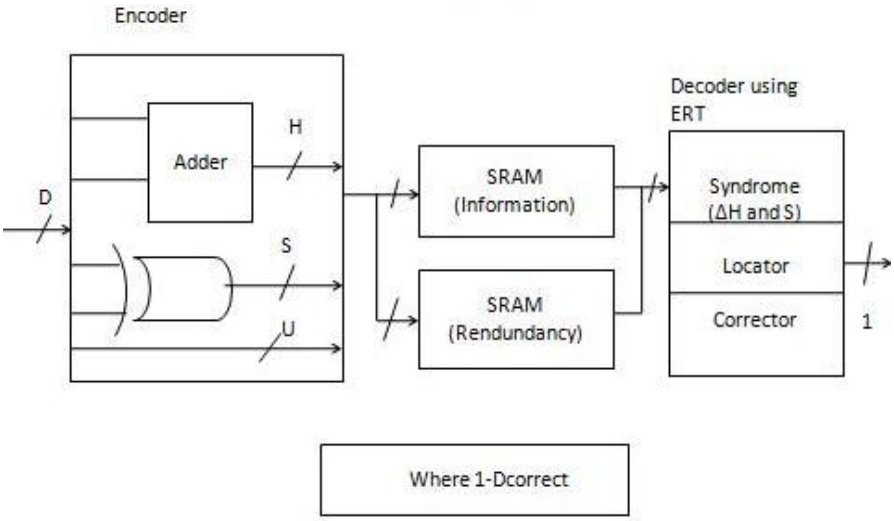
I. INTRODUCTION

AS the CMOS technology scales down to nano scale and memories are combined with an increasing the number of electronic systems, the soft error rate in memory cells is rapidly increasing, especially when memories operate in space environments due to ionizing effects of atmospheric neutron, alpha-particle, and cosmic rays . Although a single bit upset is a major concern about memory reliability, multiple cell upsets (MCUs) have become a serious reliability concern in some memory applications . In order to make memory cells as fault-tolerant as possible, some error correction codes (ECCs) have been widely used to protect memories against soft errors for years.The Bose– Chaudhuri–Hocquenghem codes Reed–solomen codes,and punctured difference set (PDS) codes have been used to deal with MCUs in memories. But these codes require more area, power, and delay overheads since the encoding and decoding circuits are more complex in these complicated codes. Interleaving technique has been used to restrain MCUs which rearrange cells in the physical arrangement to separate the bits in the same logical word into different physical words. However, interleaving technique may not be practically used in content-addressable memory (CAM), because of the tight coupling of hardware structures from both cells and comparison circuit structures. Built-in current sensors (BICS) are proposed to assist with single-error correction and double-error detection codes to provide protection against MCUs However, this technique can only correct two errors in a word.

More recently, in 2D matrix codes (MCs) are proposed to efficiently correct MCUs per word with a low decoding delay, in which one word is divided into multiple rows and multiple columns in logical. The bits per row are protected by Hamming code, while parity code is added in each column. For the MC based on Hamming, when two errors are detected by Hamming, the vertical syndrome bits are activated so that these two errors can be corrected. As a result, MC is capable of correcting only two errors in all cases. In an approach that combines decimal algorithm with Hamming code has been conceived to be applied at software level. It uses addition of integer values to detect and correct soft errors. The results obtained have shown that this approach have a lower delay overhead over other codes. The advantage of decimal algorithm is that the error detection capability is maximized so that the reliability of memory is the enhanced. Besides, the encoder-reuse technique (ERT) is proposed to minimize the area overhead of extra circuits (encoder and decoder) without disturbing the whole encoding and decoding processes, because the ERT uses DMC encoder itself to be part of the decoder. The proposed DMC is the introduced and its encoder and decoder circuits are present in Section two. The section also illustrates the limits of simple binary error. detection and the advantage of decimal error detection. The reliability and overheads analysis of the proposed code are analyzed in Section three. The Section four, the implementation of decimal error detection together with BICS for error correction in CAM is provided.

II-PROPOSED DMC

DMC is proposed to assure reliability in the presence of MCUs with reduced performance overheads, and a 32-bit word is encoded and decoded based on the proposed techniques.



Proposed Schematic of Fault-Tolerant Memory Protected with DMC

A. Proposed Schematic of the Fault-Tolerant Memory

The proposed schematic of the fault-tolerant memory is depicted . First, during the encoding (write) process, information bits D are fed to the DMC encoder, and then the horizontal redundant bits H and the vertical redundant bits V are obtained from the DMC encoder. When the encoding process is completed, the obtained DMC code word is stored in the memory. If MCUs occur in the memory, these the errors can be corrected in the decoding (read) the process. Due to the advantage of decimal algorithm, the proposed DMC has higher fault-tolerant capability with the lower performance overheads. In the fault-tolerant memory, the ERT technique is proposed to reduce the area overhead of extra circuits and will be introduced in the following sections.

B. Proposed DMC Encoder

In the proposed DMC, first, the divide-symbol and arrange-matrix ideas are performed, i.e., the N-bit the word is divided into k symbols of m bits (N = k × m), and these symbols are arranged in a k1 × k2 2-D matrix (k = k1 × k2, where the values of k1 and k2 represent the numbers of rows and the columns in the logical matrix respectively). Second, the horizontal redundant bits H are produced by performing the decimal integer addition of the selected symbols per row. Here, each symbol is regarded as a decimal integer. Third, the vertical redundant bits V are obtained by the binary operation among the bits per column. It should be noted that both the divide-symbol and arrange-matrix are implemented in logical instead of in physical.

Therefore, the proposed DMC does not require to changing the physical structure of the memory. To explain the proposed DMC scheme, we take a 32-bit word. The cells from D0 to D31 are information bits. This 32-bit word has been divided into eight symbols of 4-bit. k1 = 2 and k2 = 4 have been chosen simultaneously. H0–H19 are horizontal check bits V0 through V15 are vertical the check bits.

However, it should be mentioned that the maximum correction capability (i.e., the maximum size of the MCUs can be corrected) and the number of redundant bits are different when the different values for k and m are chosen. Therefore, k and m should be carefully adjusted to maximize the correction capability and minimize the number of redundant bits The horizontal redundant bits H can be obtained by decimal integer addition as follows:

$$H4H3H2H1H0 = D3D2D1D0 + D11D10D9D8$$
$$H9H8H7H6H5 = D7D6D5D4 + D15D14D13D12$$

and the similarly for the horizontal redundant bits H14H13H12H11H10 and H19H18H17H16H15, where "+" represents decimal integer addition. For the vertical redundant bits V, and we have

$V0 = D0 \oplus D16$

$V1 = D1 \oplus D17$

and the similarly for the rest vertical redundant bits. The encoding can be performed by the decimal and binary addition operations from (1) to (4). The encoder that computes the redundant bits using multibit adders and XOR gates . The figure, H19 − H0 are horizontal redundant bits, V15 − V0 are vertical redundant the bits, and the remaining bits U31 − U0 are the information bits which are directly copied from D31 to D0. The enable signal En will be explained in the next section.

C. Proposed DMC Decoder

To obtain a word being corrected, and the decoding process is required. first, received the redundant bits H4H3H2H1H'0andV'0−V'3 are generated by the received information bits D'. Second, the horizontal syndrome bitsH4H3H2H1H0 and the vertical syndrome bits S3 − S0 can be calculated as follows:

$$H4H3H2H1H0 = H4H3H2H1H'0 - H4H3H2H1H0$$

$S0 = V'0 \oplus V0$ and similarly for the rest vertical syndrome bits, where "−"represents decimal integer subtraction. The decoding process: syndrome calculator, error locator, and error corrector. It can be observed from this figure that the redundant bits must be recomputed from the received information bits D' and compared to the original set of the redundant bits in order to obtain the syndrome bits H and S.

Then error locator uses H and S to detect and locate which bits the some of the errors occur in. Finally, in the error corrector, these errors can be corrected by inverting the values of error bits. The proposed scheme, the circuit area of DMC is minimized by reusing its encoder. This is called the ERT.the DMC encoder is also reused for obtaining the syndrome bits in the DMC decoder. Therefore, the whole circuit area of DMC can be minimized as a result of using the existent circuits of the encoder. Besides, this figure also shows the proposed a decoder with an enable signal En for deciding whether the encoder it needs to be a part of the decoder. In other words, the En signal is used for distinguishing the encoder from the decoder, and it is under the control of the write and read the signals in a memory.

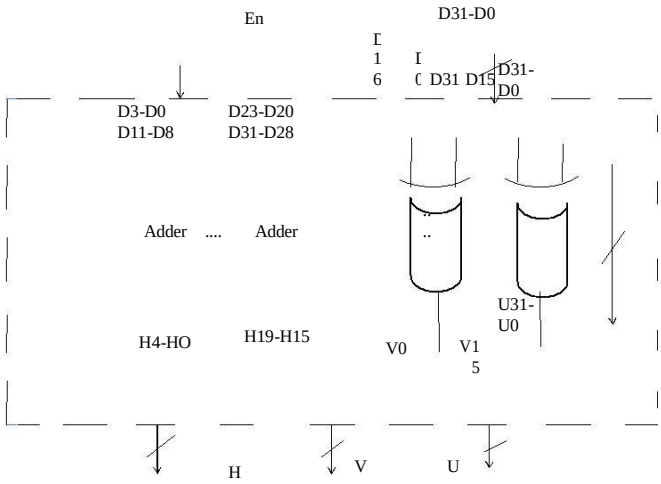
Therefore, in the encoding (write) process, the DMC encoder is only an encoder to execute the encoding a operations. However, in the decoding (read) process, this encoder is employed for computing the syndrome bits in the decoder. These clearly show how the area overhead of an extra circuits can be substantially reduced.

E. Advantage of Decimal Error Detection

The error detection based on binary algorithm can only detect a finite number of errors. However, when the decimal algorithm is used to detect errors, these errors can be detected so that the decoding error can avoided. The reason is that the operation mechanism of decimal algorithm is different from that of binary. The detection procedure of decimal error detection using the proposed structure is fully described. First of all, the horizontal redundant bits H4H3H2H1H0 are obtained from the original information bits in symbols 0 and 2 according to:

H4H3H2H1H0
=D3D2D1D0 +D11D10D9D8
= 1100 + 0110
= 10010.

H4H3H2H1H0
=D3D2D1D0 +D11D10D9D8
= 1100 + 0110
=10010.



When MCUs occur in symbol 0 and symbol 2, i.e., the bits in symbol 0 are upset to "1111" from "1100" (D3D2D1D'0 = 1111) and the bits in symbol 2 are upset to "0111" from "0110" (D11D10D9D'8 = 0111). During the decoding process, the received horizontal redundant bits H4H3H2H1H'0 are first computed, as follows:

H4H3H2H1H'0
= D11D10D9D'8+ D3D2D1D'0
= 0111 + 1111
= 10110.

Then, the horizontal syndrome bits ΔH4H3H2H1H0 can be obtained using decimal integer subtraction

ΔH4H3H2H1H0

= H4H3H2H1H'0−H4H3H2H1H0
= 10110 – 10010
= 00100.

The decimal value of ΔH4H3H2H1H0 is not "0," which represents that errors are detected and located in symbol 0 or symbol 2. Subsequently, the precise location of the bits that were flipped can be located by using the vertical syndrome bits S3 − S0 and S11 − S8. Finally, all these errors can be corrected by. Therefore, based on decimal algorithm, the proposed technique has higher tolerance capability for protecting memory against MCUs. As a result, it is possible that all single and double errors and any types of multiple errors per row can be corrected by the proposed technique no matter whether these errors are consecutive or inconsecutive.

V. CONCLUSION

In this paper, novel per-word DMC was proposed to assure the reliability of memory. The proposed protection code utilized decimal algorithm to detect the errors, so that more errors were detected and corrected. The obtained results showed that the proposed scheme has a superior of the protection level against large MCUs in memory. Besides, the proposed decimal error detection technique is an attractive the opinion to detect MCUs in CAM because it can be combined with the BICS to provide an adequate level of immunity. The only drawback of the proposed DMC is that more redundant bits are required to maintain the higher reliability of memory, so that a reasonable combination of k and m should be chosen to maximize memory reliability and minimize the number of redundant bits based on radiation experiments in actual implementation

FUTURE WORK:.

Therefore, future work will be conducted for the reduction of the redundant bits and the maintenance of the reliability of the proposed technique

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